WHAT IS CLAIMED IS:

1. An SRAM-compatible memory having a plurality of memory banks each having a plurality of DRAM cells arranged in a matrix form defined by rows and columns, the SRAM-compatible memory interfacing with an external system in which no timing period is externally set for a refresh operation of the DRAM cells, comprising:

the plurality of memory banks for storing input data in DRAM cells specified by an input address externally provided, wherein write operations of the memory banks are independently controlled such that when a refresh operation or a write operation for a previous frame is being performed in a certain memory bank, write operation of input data is independently performed with respect to the respective memory banks except for the certain memory bank;

a parity generator for generating an input parity based on the input data, the input parity having a certain preset parity value in conjunction with the input data; and

a parity bank for storing the input parity.

2. The SRAM-compatible memory as set forth in claim 1, further comprising:

a plurality of bank control units for controlling the refresh operation and the write operation of the memory banks, each of the bank control units being associated with corresponding one of the memory banks; and

a parity control unit for controlling the refresh operation and the write operation of the parity bank.

3. The SRAM-compatible memory as set forth in claim 2, wherein the bank control units each including;

a data buffer for storing input data whose write operation in a memory bank is suspended due to a refresh operation or a write operation for a previous frame in the memory bank; and

an address buffer for storing input address designating DRAM cells of the memory bank.

4. The SRAM-compatible memory as set forth in claim 3, wherein the data buffer provides the input data stored therein to the memory bank after the refresh operation or the write operation is completed, and the address buffer provides the input address stored therein to the memory bank after the refresh operation or the write operation is completed.

5. The SRAM-compatible memory as set forth in claim 2, further comprising a refresh address generator for generating a refresh address to designate DRAM cells of the memory banks to be refreshed.

6. The SRAM-compatible memory as set forth in claim 5, wherein each of the bank control units further comprises an address selector for selecting one of the input address and the refresh address and providing the selected address to corresponding one of the memory banks to perform the write operation or the refresh operation with respect to DRAM cells in the corresponding one of the memory banks.

7. The SRAM-compatible memory as set forth in claim 2, further comprising a flag generator for generating a refresh flag signal to the respective bank control units, each of the bank control units controlling the refresh operation in corresponding one of the memory banks in response to the refresh flag signal.

8. The SRAM-compatible memory as set forth in claim 7, wherein the flag generator generates a refresh driving signal which is periodically activated, the refresh driving signal controlling a refresh address generator to generate a refresh address to designate DRAM calls of the memory banks to be refreshed.

9. The SRAM-compatible memory as set forth in claim 8, wherein the refresh address is changed in response to a predetermined number of activations of the refresh driving signal.

10. The SRAM-compatible memory as set forth in claim 9, further comprising a refresh timer for generating a refresh request signal to the flag generator, the refresh driving signal being activated in response to the refresh request signal.

11. The SRAM-compatible memory as set forth in claim 2, wherein the parity bank has a substantially same structure as each of the memory banks.

12. A method of driving an SRAM-compatible memory having a plurality of memory banks each having a plurality of DRAM cells arranged in a matrix form defined by rows and columns, the SRAM-compatible memory interfacing with an

external system in which no timing period is externally set for a refresh operation of the DRAM cells, comprising:

providing multiple pieces of input data to the memory banks, each piece of the input data being provided to corresponding one of the memory banks;

determining whether a refresh operation or a write operation for a previous frame is being performed in the memory banks;

storing a piece of the input data in a data buffer if the refresh operation or the write operation is being performed in a certain memory bank, wherein the piece of the input data is provided to the certain memory bank and write operation of the piece of the input data is suspended; and

writing the piece of the input data stored in the data buffer into DRAM cells of the certain memory bank after the refresh operation or the write operation is completed;

wherein the memory banks except for the certain memory bank independently perform write operations, while the refresh operation or the write operation for the previous frame is performed with respect to the certain memory bank.

13. The method as set forth in claim 12, further comprising:

obtaining an input parity from a predetermined preset parity value and the input data; and

writing the input parity into a parity bank.

14. The method as set forth in claim 12, further comprising:

storing an input address designating DRAM cells in the certain memory bank into an address buffer; and

providing the input address to the certain memory bank after the refresh operation or the write operation is completed.